SYNOPSYS®

DATASHEET

PrimeECO

PrimeECO is the only ECO closure system using Primetime STA and production P&R engines that results in fewer ECO iterations

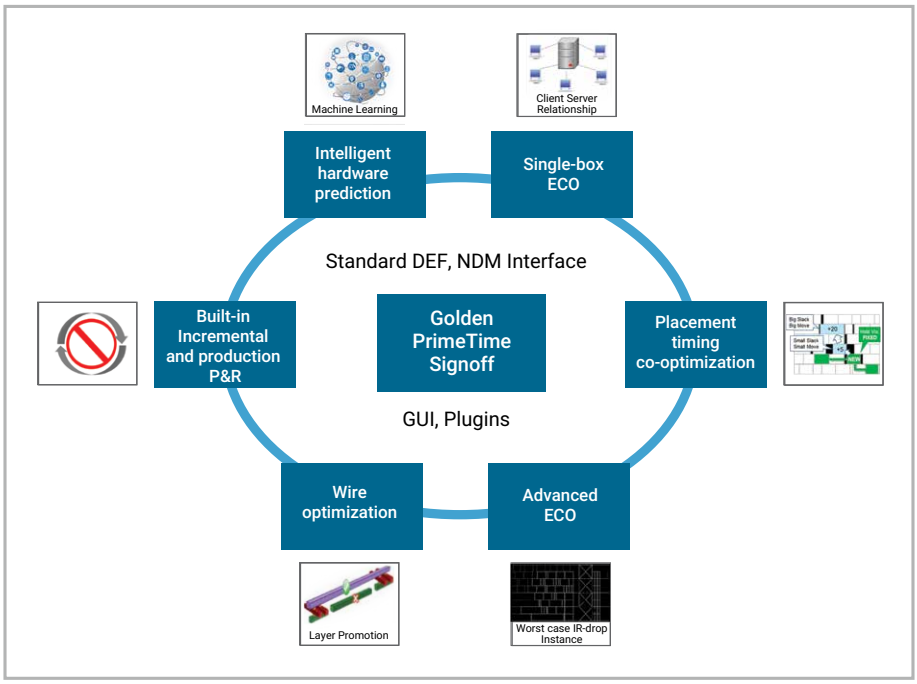
Overview

ECO has become a critical and growing component of the chip implementation mainly driven by rapidly increasing signoff scenarios and physical complexity at advanced nodes. It is already consuming 25-50% of the overall design schedule. This is caused by high number of iterations between P&R tools and ECO tools due to poor Physical/ timing correlation. On the other hand the ECO runs are highly compute intensive requiring very large number of high-capacity machines.

PrimeECO™ is the industry's first signoff-driven ECO closure solution that achieves signoff closure in a single cockpit.

Design Closure System

PrimeECO™ enables 5X faster single-machine design closure by uniquely combining the efficiency to manage unlimited signoff scenario views with the scalability of incrementally enabled, integrated physical implementation and signoff capabilities, eliminating the costly iteration between implementation and signoff.



Single-Machine Multi-Scenario Closure with Hybrid Timing View

The PrimeECO solution features an innovative, machine-learning driven Hybrid Timing View technology that addresses the increasing signoff scenarios by predicting optimal trade-offs between required compute resource and desired timing accuracy. The Hybrid Timing View deploys PrimeTime® signoff engine for real-time updates on accuracy-critical scenarios, while ensuring complete visibility on coverage-critical scenarios through efficient static views. The outstanding efficiency of Hybrid Timing View enables thousands of timing scenarios to be loaded onto a single box, eliminating the need for large number of compute resources typically required for signoff coverage.

Common Data Model with Fusion Design Platform

To further eliminate design iterations, the PrimeECO solution is architected on the Synopsys Fusion Design™ Platform, the world's first artificial-intelligence (AI) enhanced, cloud-ready design platform, with direct access to incrementally enabled placement, routing, extraction, physical verification and signoff technologies from Synopsys' market-leading portfolio of solutions, including IC Compiler™ II, Fusion Compiler™, IC Validator, StarRC™, PrimeTime, PrimePower, and PrimeYield. Within this single-environment design closure cockpit, not only is every change fully implemented and validated, but it also creates new opportunities for placement, routing, and timing co-optimization to achieve power, performance and area (PPA) results previously impossible in traditional design closure flows.

Unique Graphical User Interface with Exclusive Signoff Timing Overlay

The PrimeECO solution is the industry's only design closure solution with access to PrimeTime golden signoff results. An intuitive cockpit provides a unique graphical user interface to overlay Hybrid Timing View on design visualization for final touch-ups, including an open database interface available to custom scripts for user-driven optimization. The exclusive PrimeECO solution is available to all designers innovating on the Fusion Design Platform as well as industry-standard DEF databases.

Benefits

The PrimeECO solution is the only ECO closure solution with production timing and P&R engines. Here is the summary of benefits:

- Signoff accuracy with access to PrimeTime golden signoff results
- Full chip capacity—Can process blocks, subchips as well as chip level ECO
- Support for signoff scenarios—Hundreds of scenarios handled efficiently with its Hybrid view feature
- Complete ECO jobs with less compute resource—2-5X Less number of cores required and 2-5X less memory per machine required
- Superior ECO QoR (fix-rates) with timing-P&R co-optimization capability
- Fewer ECO iterations using production P&R engines
- Incremental ECO

OS Platform Support

PrimeECO supports:

- RHEL 6.6+, 7.x, 8+
- CentOS 6.6+, 7.1.1503+, 8+
- SLES 12+, 15+

See the Synopsys Release Specific Support documents for further details.